METHOD AND SYSTEM FOR REDUCING CHARGE DAMAGE IN SILICON ON INSULATOR TECHNOLOGY

ABSTRACT OF THE DISCLOSURE

According to one embodiment of the invention, a silicon-on-insulator device includes an insulative layer formed overlying a substrate and a source and drain region formed overlying the insulative layer. The source region and the drain region comprise a material having a first conductivity type. A body region is disposed between the source region and the drain region and overlying the insulative layer. The body region comprises a material having a second conductivity type. A gate insulative layer overlies the body region. This device also includes a gate region overlying the gate insulative layer. The device also includes a diode circuit conductively coupled to the source region and a conductive connection coupling the gate region to the diode circuit.